The Guidance to Become a RAN Engineer

P10942A10 **Huang Hsu-Hong**

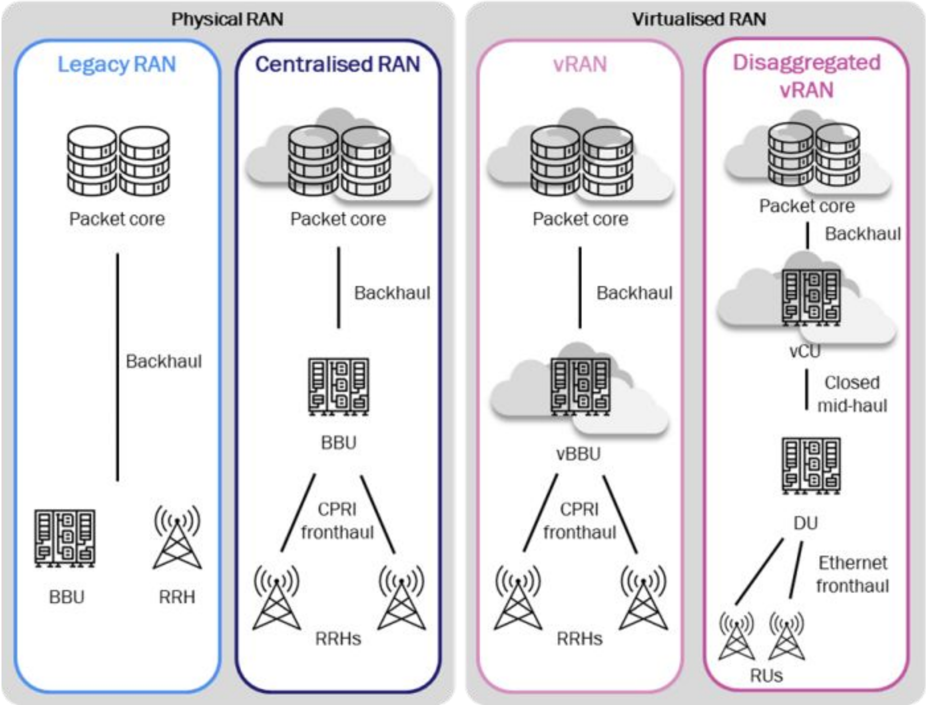
Wireless Mobile Network Laboratory
of National Taiwan University

Agenda

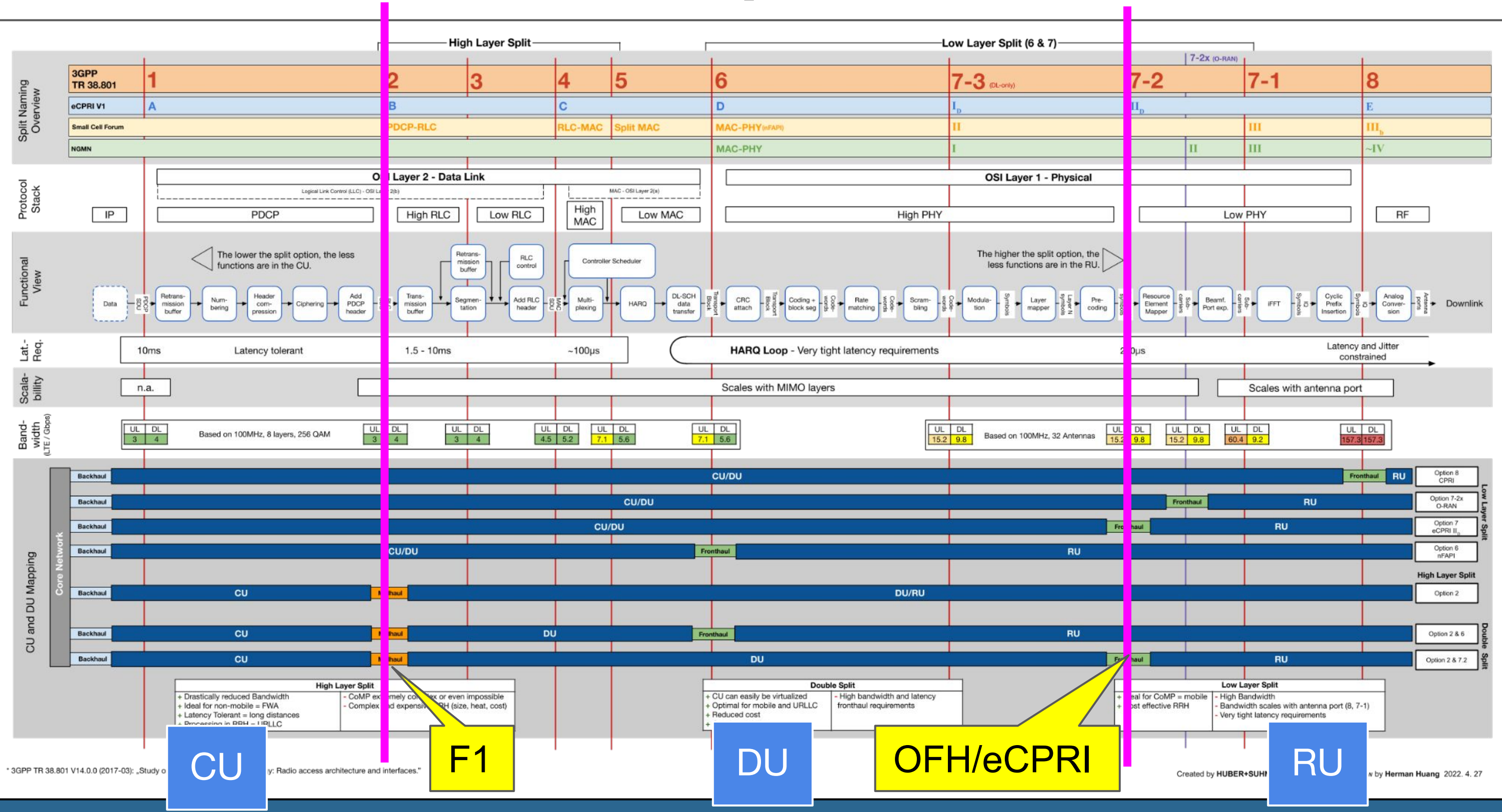
1. **Part I: RAN Retrospect**
2. **Part II: Handmade RAN**
    a. PTP(Precise TIme Prorocol): IEEE 1588V2/SyncE
3. **Part III: Specialized Knowledge**
    a. Linux Programming
    b. DPDK
    c. QAT Encrypt/Decrypt

Part I: RAN Retrospect

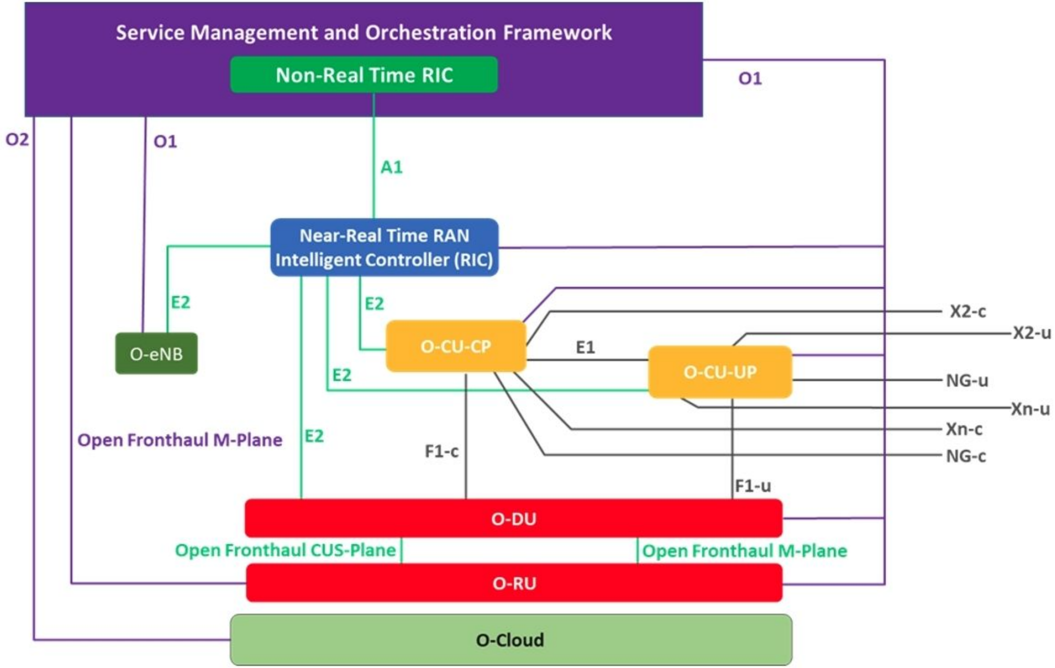
The Evolution of RAN Architecture



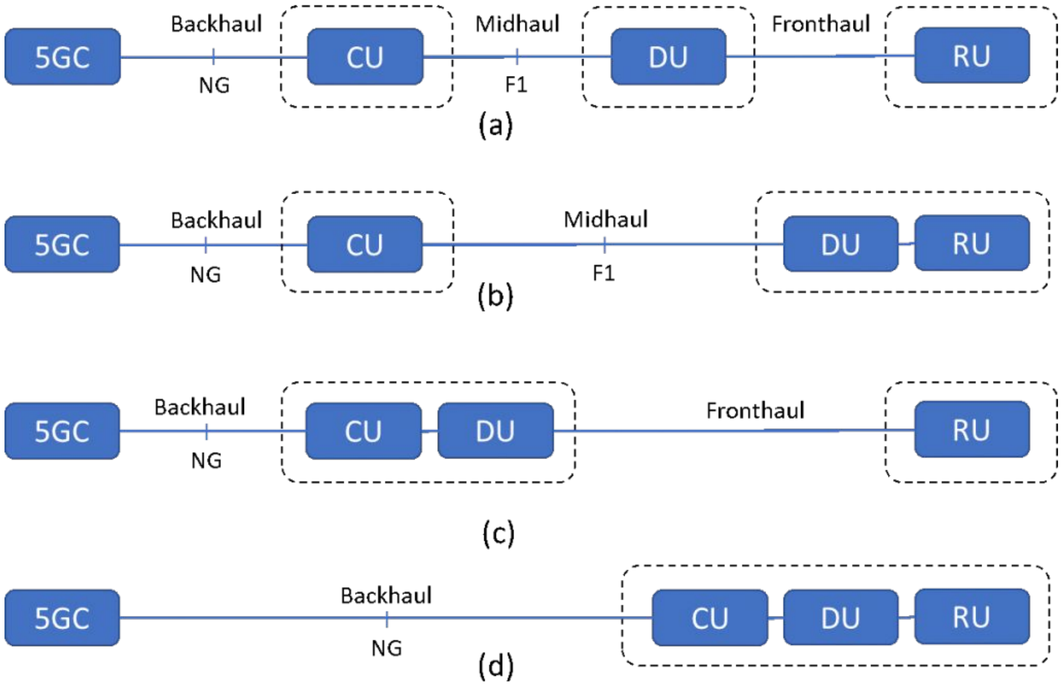
Functional Split Overview



O-RAN Logical Architecture

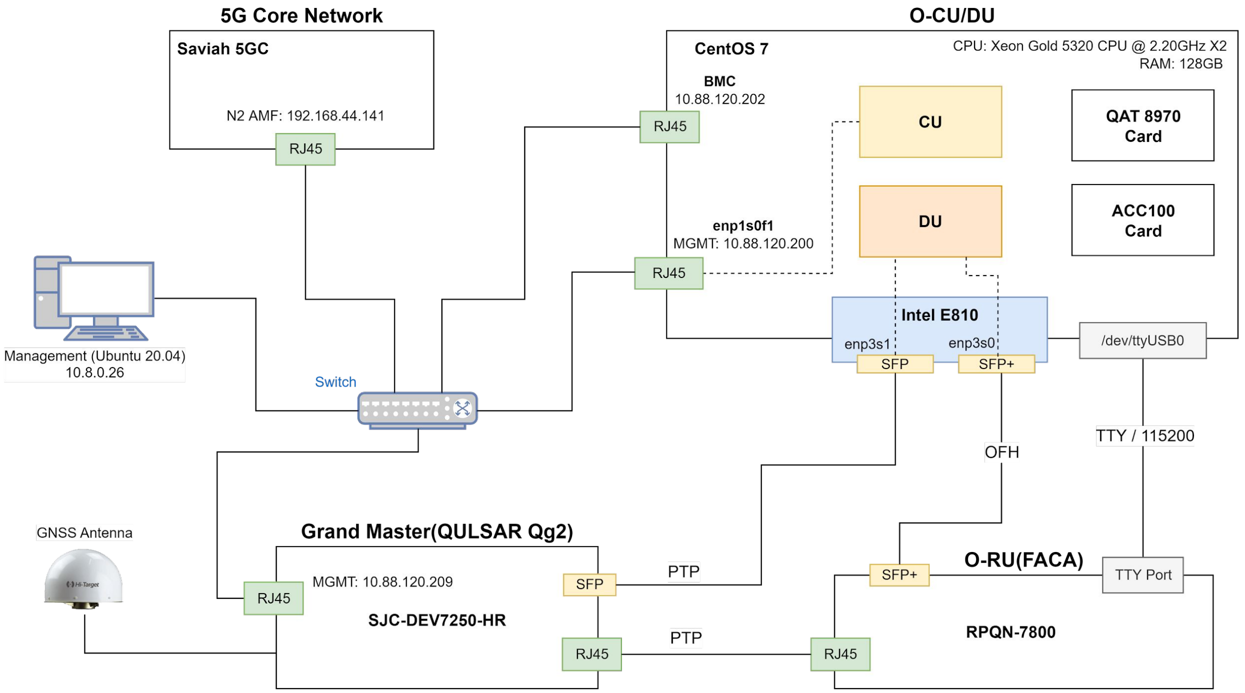


Backhaul, Midhaul, and Fronthaul

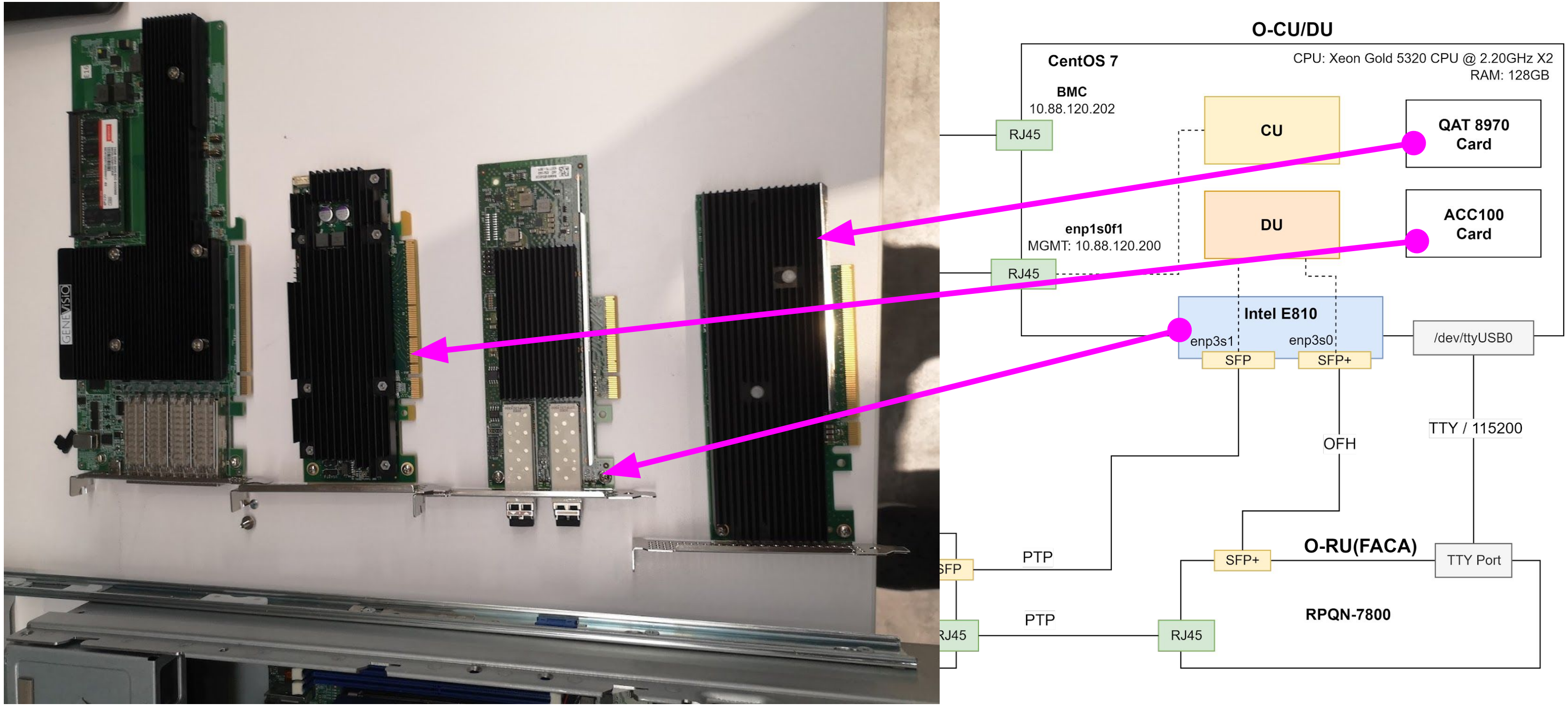


Part II: Handmade RAN

O-RAN System Archtecture



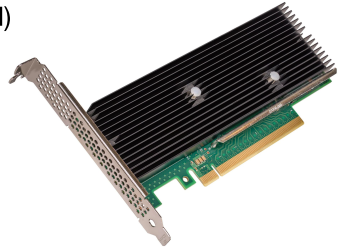
Accelerator Cards

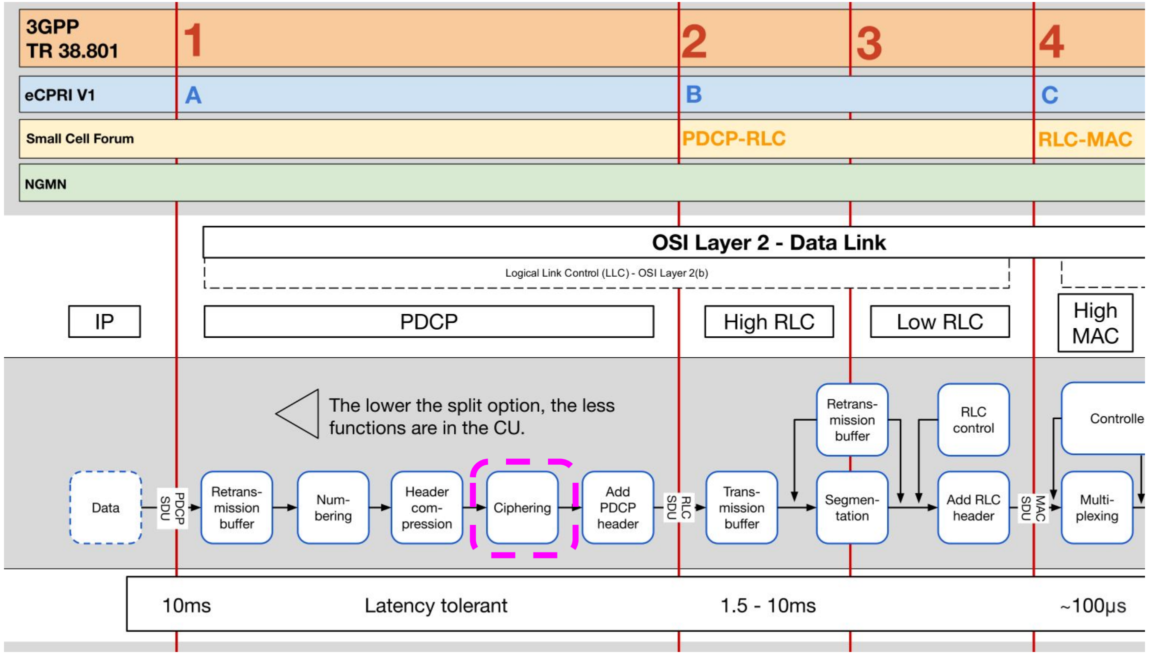


PDCP Ciphering Accelerator Card

Intel® QuickAssist Adapter 8970

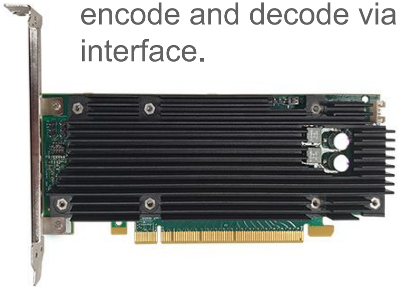
- Ciphers (AES, 3DES/DES, RC4, KASUMI, ZUC, Snow 3G)
- Message digest/hash (MD5, SHA-1, SHA-2, SHA-3) and authentication (HMAC, AES-XCBC)
- Algorithm chaining (one cipher and one hash in a single operation)
- Authenticated encryption (AES-GCM, AES-CCM)
- AES-XTS

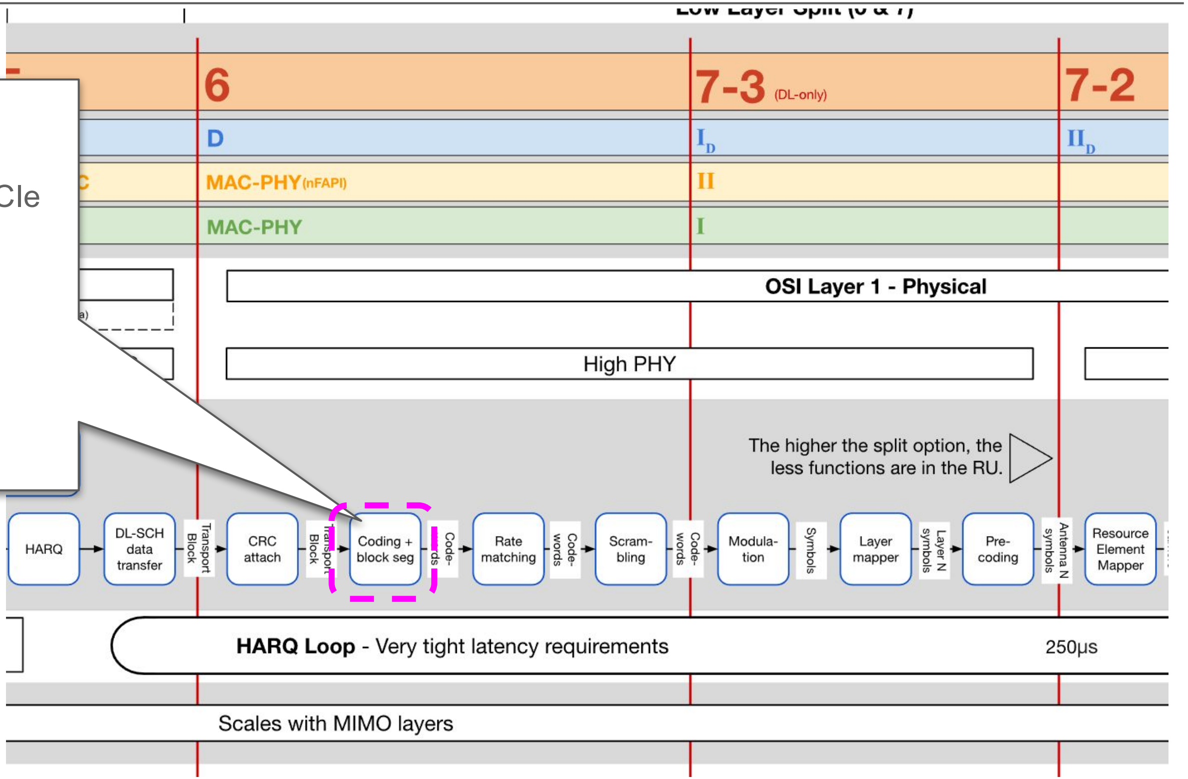




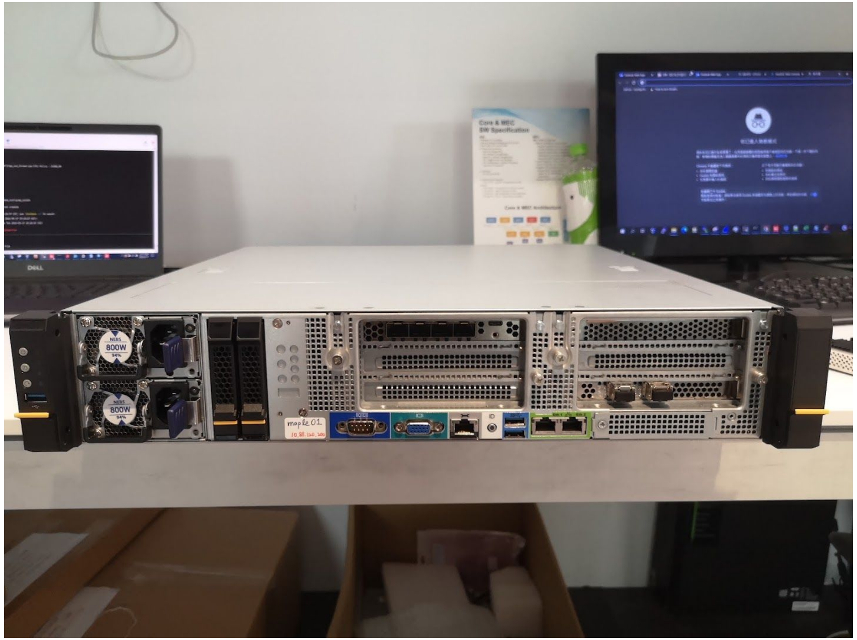
High PHY Accelerator Card

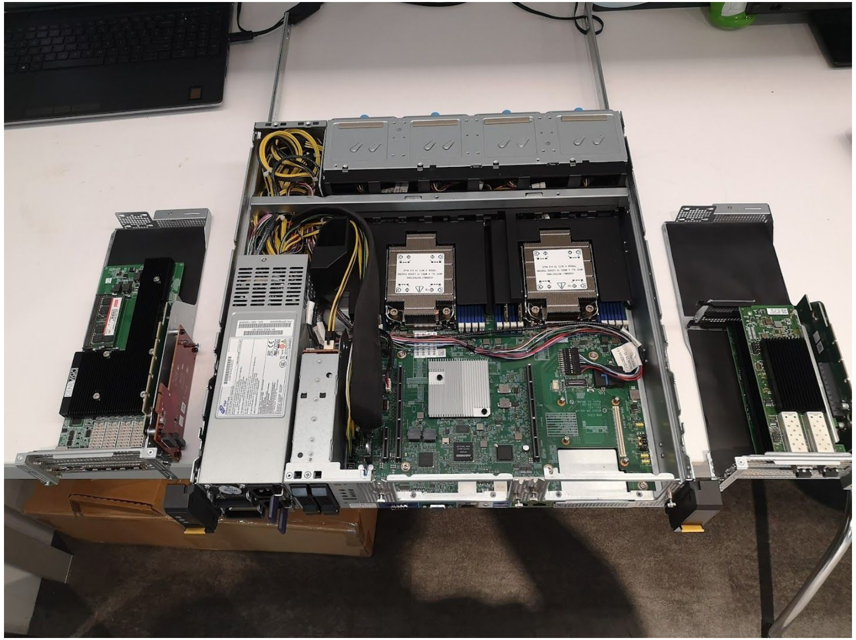
The ACC100 provides 4G (**Turbo**) and 5G (**LDPC**) encode and decode via PCIe interface.



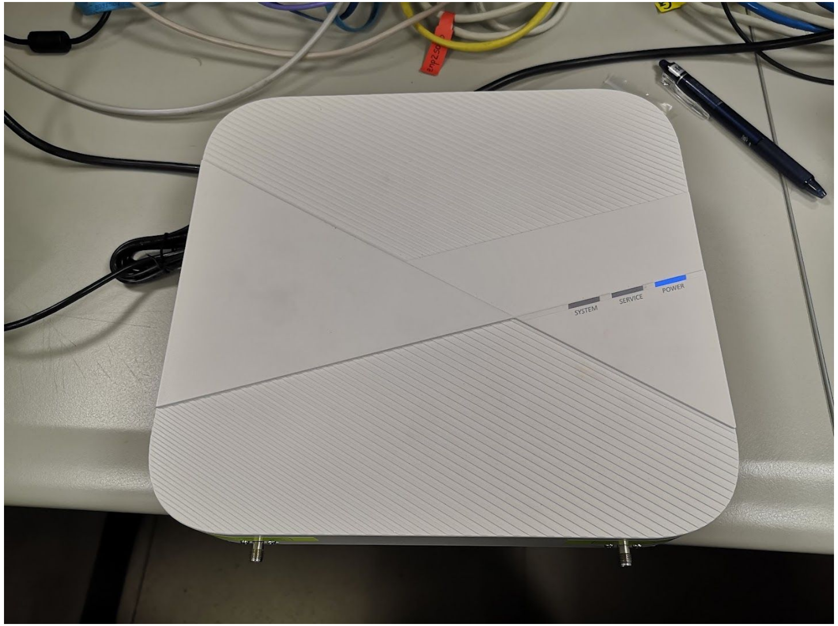


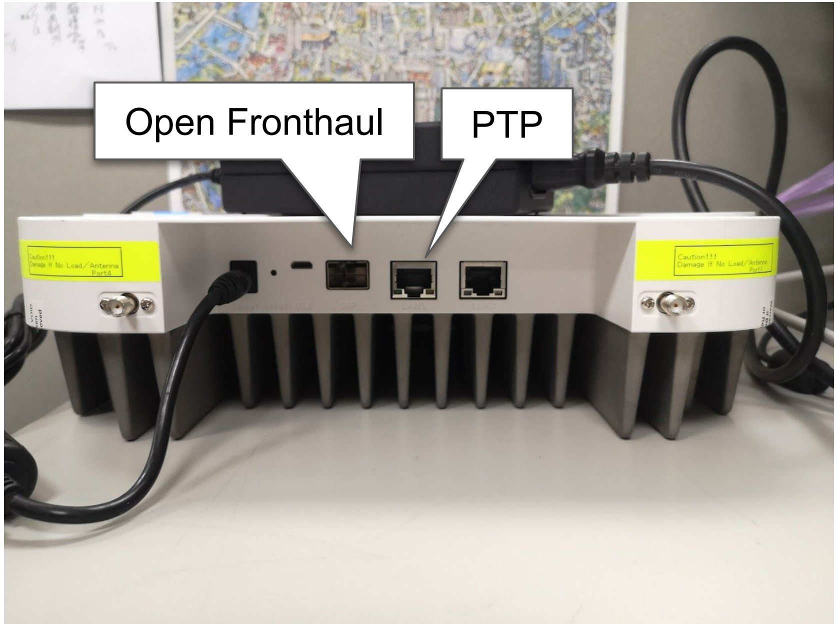
X86 Server



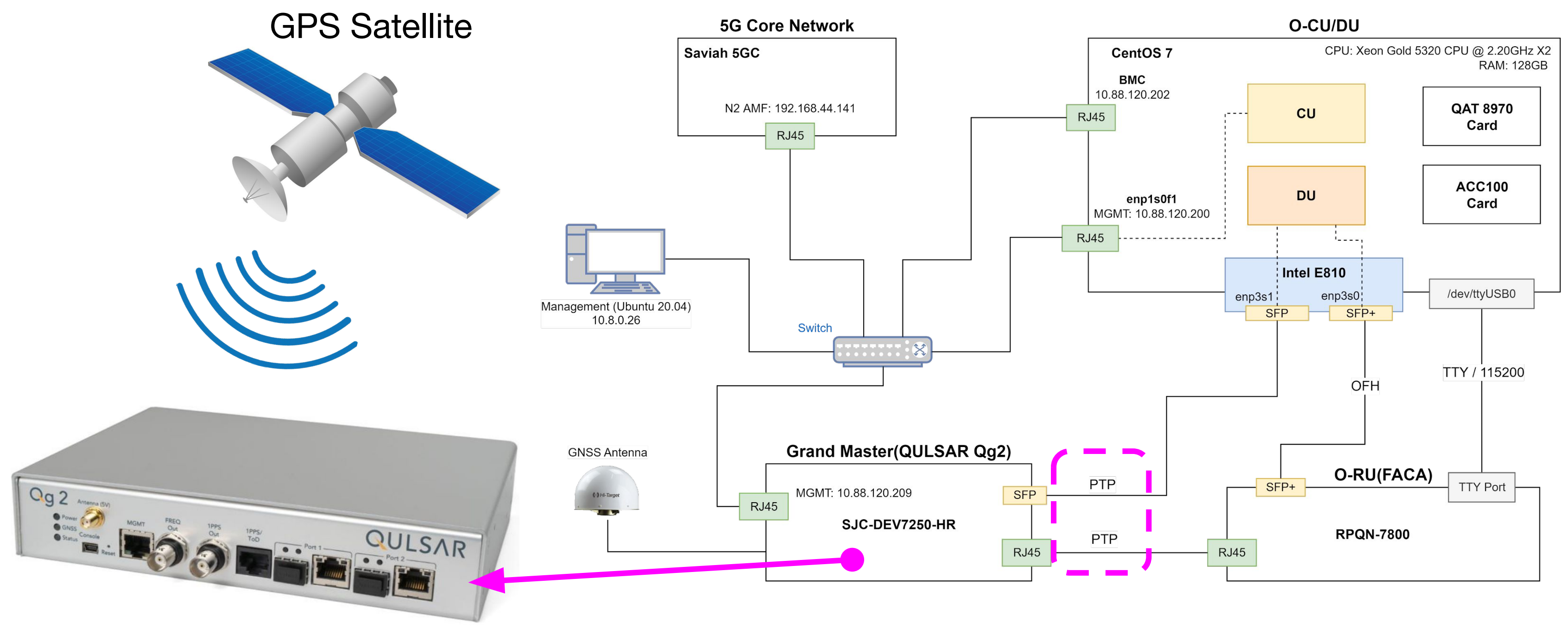


RU





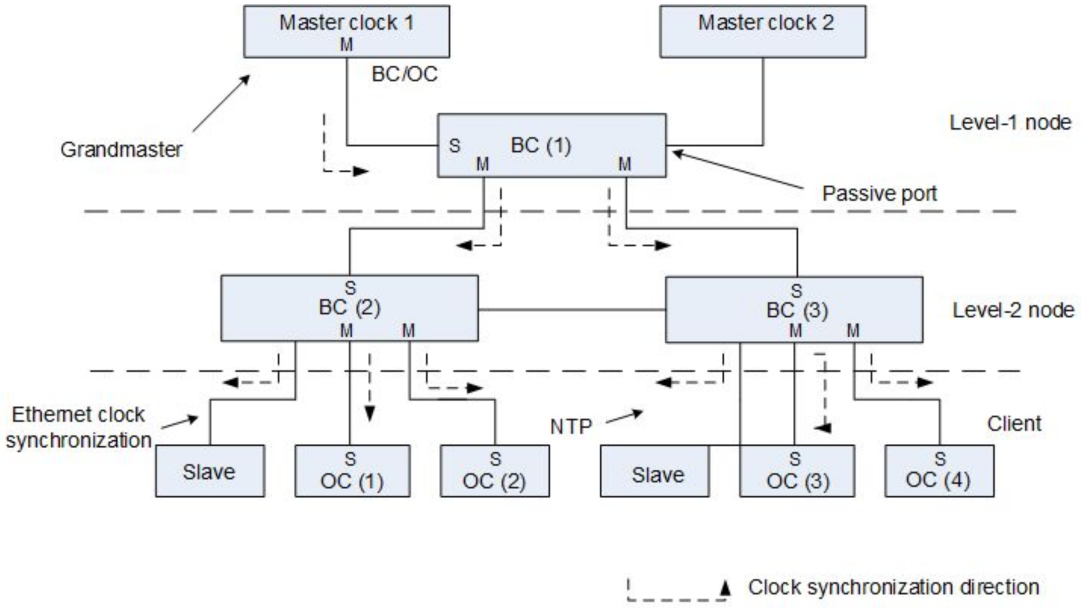
PTP (Precise TIme Prorocol)



Clock Synchronization Network Hierarchy

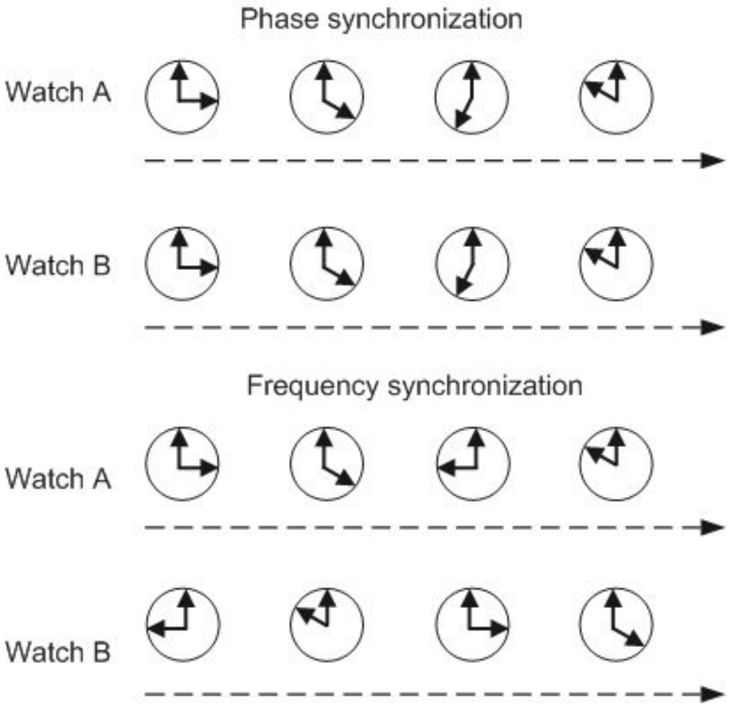
- **Ordinary clock (OC)**: has a **single PTP port** in a domain and maintains the timescale used in the domain It may and maintains the timescale used in the domain. It may serve as a source of time, i.e., be a master, or may synchronize to another clock, i.e., be a slave.

- **Boundary clock (BC)**: has **multiple PTP ports** in a domain and maintains the timescale used in the domain. A boundary clock in PTP is **both a slave and a master** clock. It will take the timing message in, adjust for delay, and then create a *new* master time signal to pass down the network. .

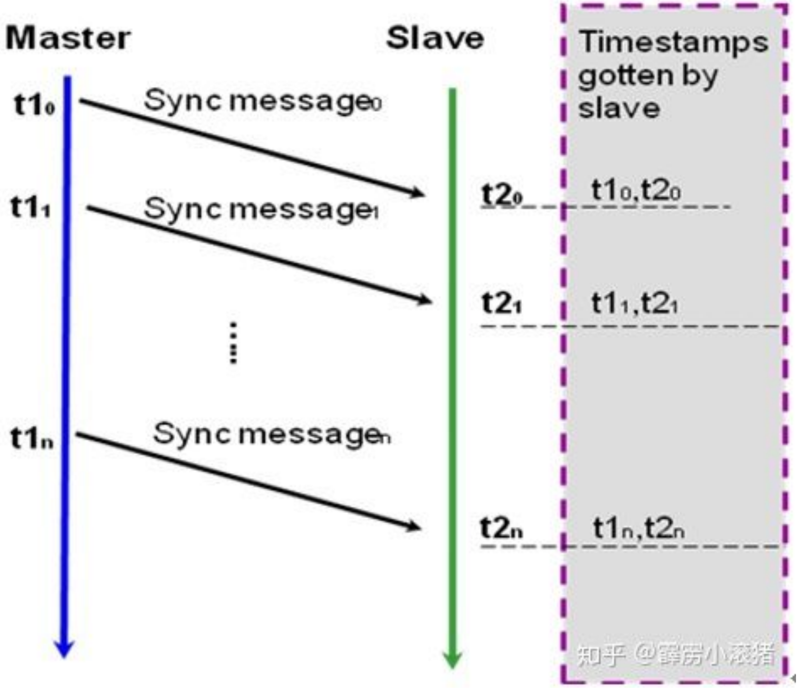


Synchronization

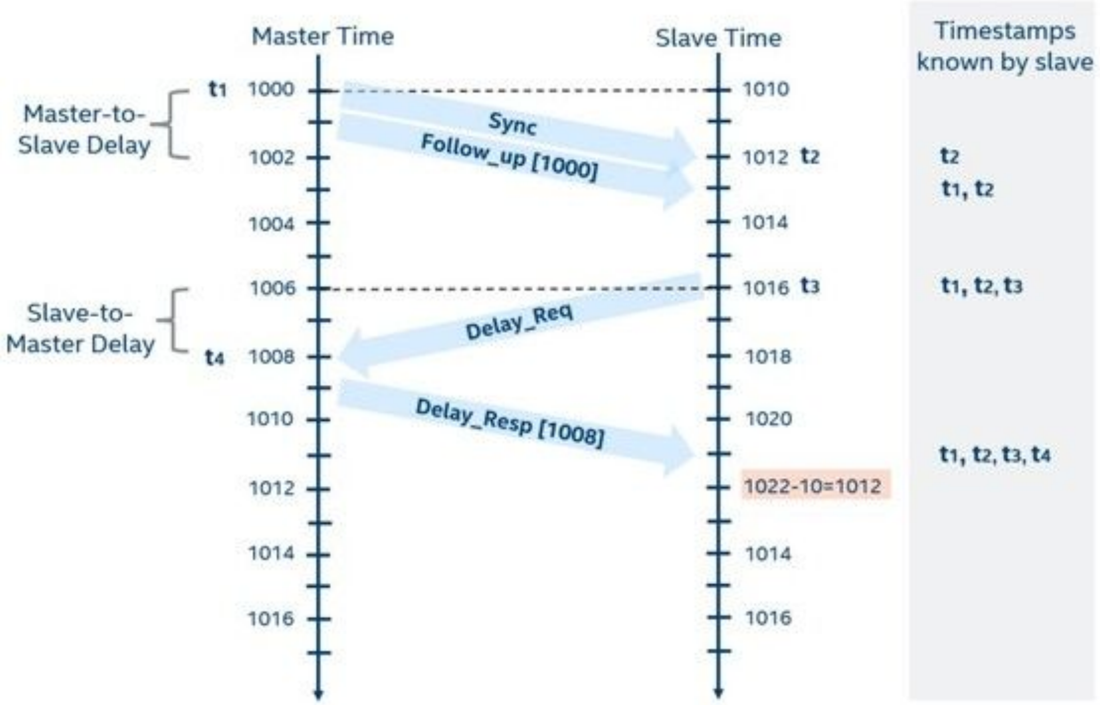
- **Time synchronization, also called phase** synchronization, means that both the frequency of and the time between signals remain constant. In this case, the time offset between signals is always 0.
- **Frequency synchronization, also called clock synchronization,** refers to a constant frequency offset or phase offset. In this case, signals are transmitted at a constant average rate during any given time period so that all the devices on the network can work at the same rate.



Frequency synchronization



Time synchronization



Delay = $[(t_2 - t_1) + (t_4 - t_3)] / 2$
Offset = $(t_2 - t_1)$ - Delay

$t_1 = 1000$
$t_2 = 1012$
$t_3 = 1016$
$t_4 = 1008$

Assuming symmetrical path delay:
Path Delay
$= [(t_2 - t_1) + (t_4 - t_3)] / 2$
$= [(1012 - 1000) + (1008 - 1016)] / 2$
$= [12 + (-8)] / 2$
$= 2$

Offset from Master Clock
$= (t_2 - t_1)$ - Delay
$= (1012 - 1000) - 2$
$= 12 - 2$
$= 10$

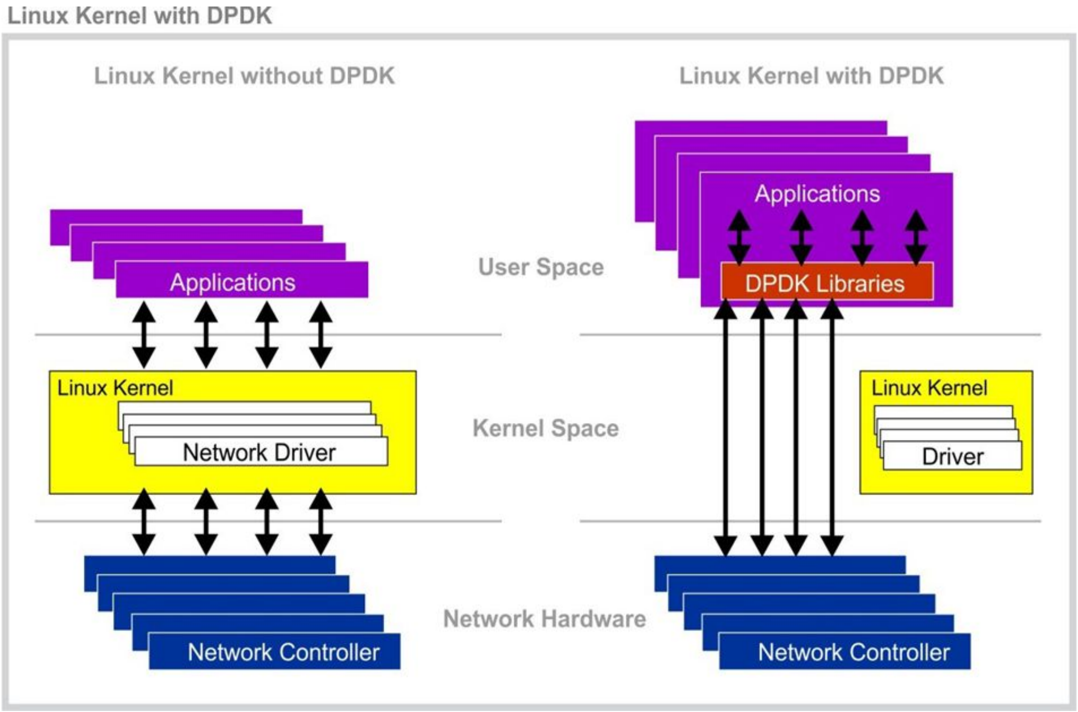
Part III: Specialized Knowledge

Linux Programming

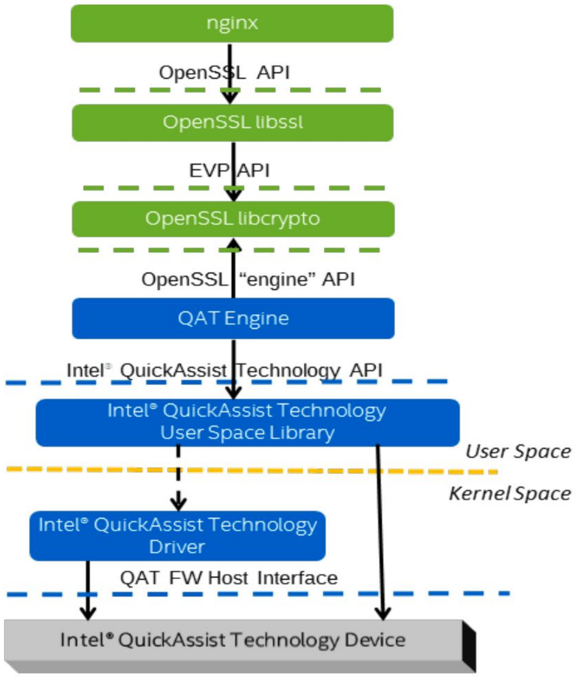
1. Linux
    1.1. Install Linux in a real machine
    1.2. Live in the Command Line
        1.2.1. Account, Permission,
        1.2.2. Networking
        1.2.3. ssh, tmux
        1.2.4. VIM…
        1.2.5. awk、sed、regular expression、Bash
    1.3. Kernel Module Installation
    1.4. boot, GRUB
    1.5. Kernel Parameters
    1.6. BPF(Berkeley Packet Filter), eBPF
2. Programming
    2.1. C Programming: gcc, Makefile
    2.2. Debug Tools: gdb, valgrind
    2.3. Makefile
    2.4. Socket Programming
    2.5. IPC: socket、signal、pipe、share memory, queue…
    2.6. Library Usage
    2.7. Kernel Module Programming
    2.8. C++ Programming
    2.9. Linux From Scratch

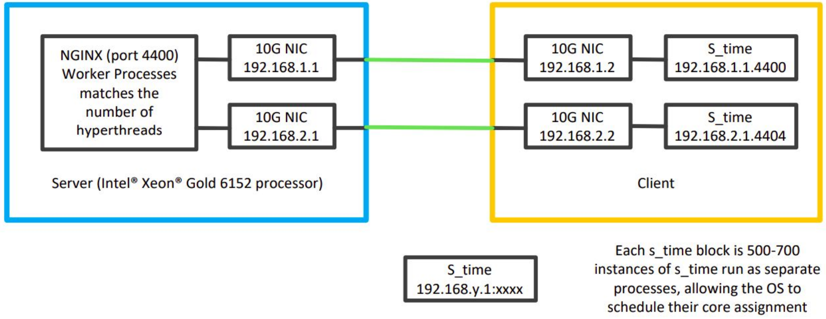
DPDK

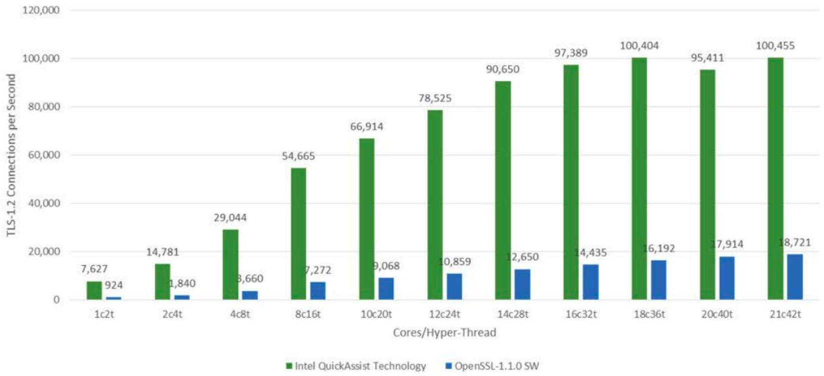
The DPDK libraries allow **direct access to the hardware without using the Linux kernel**. The data plane processing is handled by the DPDK libraries that pass network packets directly to the application network stack without any Linux kernel overhead.



Intel QAT Programming







Thanks